

SEMICONDUCTOR MEMORY DEVICE

CROSS REFERENCE TO RELATED APPLICATION

[01] This application is a continuation of prior U.S. patent application no. 09/964,851, filed September 28, 2001, which claims the benefit of priority under 35 U.S.C. § 119 to Japanese Patent Application No. 2001-220461 filed on July 19, 2001, the entire contents of which are incorporated by reference herein.

BACKGROUND OF THE INVENTION

Field of the Invention

[02] The present invention relates to a semiconductor memory device, specifically, to a semiconductor memory device having full depletion type MISFETs.

Related Background Art

[03] In a related DRAM, a memory cell is composed of an MOS transistor and a capacitor. The scale-down of the DRAM has been remarkably advanced by the adoption of a trench capacitor structure and a stacked capacitor structure. At present, the cell size of a unit memory cell is scaled down to an area of $2F \times 4F = 8F^2$, where F is a minimum feature

size. Namely, the minimum feature size F decreases with the advance of generation, and when the cell size is generally taken to be αF^2 , a coefficient α also decreases with the advance of generation. Thus, at the present of $F=0.18 \mu\text{m}$, $\alpha=8$ is realized.

[04] In order to hereafter secure the trend of cell size or chip size which is the same as before, it is demanded to satisfy $\alpha < 8$ in $F < 0.18 \mu\text{m}$ and further satisfy $\alpha < 6$ in $F < 0.13 \mu\text{m}$, and together with microfabrication, the formation of cell size of the possible small area becomes a large problem. Accordingly, various proposals for decreasing the size of the one memory cell with the one transistor and one capacitor to $6F^2$ or $4F^2$ are made. However, practical use is not easy since there are a technical difficulty that the transistor has to be a vertical type, a problem that electric interference between adjacent memory cells increases, and in addition difficulties in terms of manufacturing technology including fabrication, film formation, and the like.

[05] On the other hand, some proposals for a DRAM in which a memory cell is composed of one transistor without using a capacitor are made as mentioned below.

- [06] (1) JOHN E. LEISS et al, "dRAM Design Using the Taper-Isolated Dynamic Cell" (IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. ED-29, NO. 4, APRIL 1982, pp707-714)
- [07] (2) Japanese Patent Laid-open Publication No. H3-171768
- [08] (3) Marnix R. Tack et al, "The Multistable Charge-Controlled Memory Effect in SOI MOS Transistors at Low Temperatures" (IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 37, MAY, 1990, pp1373-1382)
- [09] (4) Hsing-jen Wann et al, "A Capacitorless DRAM Cell on SOI Substrate" (IEDM93, pp635-638)
- [10] A memory cell in the document (1) is composed of MOS transistors, each of which has a buried channel structure. Charge and discharge to/from a surface inversion layer is performed using a parasitic transistor formed at a taper portion of an element isolation insulating film to perform binary storage.
- [11] A memory cell in the document (2) uses MOS transistors which are well-isolated from each other and uses a

threshold voltage of the MOS transistor fixed by a well potential as binary data.

[12] A memory cell in the document (3) is composed of MOS transistors on an SOI substrate. A large negative voltage is applied from the SOI substrate side, and by utilizing accumulation of holes in an oxide film of a silicon layer and an interface, binary storage is performed by emitting and injecting these holes.

[13] A memory cell in the document (4) is composed of MOS transistors on an SOI substrate. The MOS transistor is one in terms of structure, but here a structure, in which a reverse conduction-type layer is formed on top of the surface of a drain diffusion region, whereby a P-MOS transistor for write and an N-MOS transistor for read are substantially combined integrally, is adopted. With a substrate region of the N-MOS transistor as a floating node, binary data are stored by its potential.

[14] However, in the document (1), the structure is complicated and the parasitic transistor is used, whereby there is a disadvantage in the controllability of its characteristic. In the document (2), the structure is simple, but it is

necessary to control potential by connecting both a drain and a source of the transistor to a signal line. Moreover, the cell size is large and rewrite bit by bit is impossible because of the well isolation. In the document (3), a potential control from the SOI substrate side is needed, and hence the rewrite bit by bit is impossible, whereby there is a difficulty in controllability. In the document (4), a special transistor structure is needed, and the memory cell requires a word line, a write bit line, a read bit line, and a purge line, whereby the number of signal lines increases.

SUMMARY OF THE INVENTION

[15] According to one aspect of the present invention, a semiconductor memory device having full depletion type MISFETs to constitute memory cells on a semiconductor substrate via an insulating film, each of the MISFETs comprising:

[16] a semiconductor layer formed on the insulating film;

[17] a source region formed in the semiconductor layer;

[18] a drain region formed apart from the source region in the semiconductor layer, the semiconductor layer between the

source region and the drain region serving as a channel body in a floating state;

[19] a main gate formed on a first side of the channel body to forms a channel in the channel body; and

[20] an auxiliary gate formed on a second side of the channel body, the second side being opposite to the first side,

[21] wherein with a state, in which the channel body is fully depleted by an electric field from the main gate and a portion of the second side of the channel body is capable of accumulating majority carriers by an electric field from the auxiliary gate, as a thermal equilibrium state,

[22] the MISFET has a first data state in which the majority carriers are accumulated in the portion of the second side of the channel body and a second data state in which the majority carriers accumulated in the portion of the second side of the channel body are emitted.

[23] According to another aspect of the invention, a semiconductor memory device having full depletion type MISFETs to constitute memory cells on a semiconductor substrate, each of the MISFETs comprising:

- [24] a pillar semiconductor portion formed on the semiconductor substrate in the form of a pillar shape;
- [25] a source region formed in one of a top portion and a bottom portion of the pillar semiconductor portion;
- [26] a drain region formed in the other of the top portion and the bottom portion of the pillar semiconductor portion and formed apart from the source region, the pillar semiconductor portion between the source region and the drain region serving as a channel body in a floating state;
- [27] a main gate formed on a first vertical face of the channel body to form a channel in the channel body; and
- [28] an auxiliary gate formed on a second vertical face of the channel body, the second vertical face being opposite to the first vertical face,
- [29] wherein with a state, in which the channel body is fully depleted by an electric field from the main gate and a portion of the second side of the channel body is capable of accumulating majority carriers by an electric field from the auxiliary gate, as a thermal equilibrium state,

- [30] the MISFET has a first data state in which the majority carriers are accumulated in the portion of the second vertical face of the channel body and a second data state in which the majority carriers accumulated in the portion of the second vertical face of the channel body are emitted.

BRIEF DESCRIPTION OF THE DRAWINGS

- [31] Fig. 1 is a sectional view showing a structure of a memory cell using a PD-type MISFET;
- [32] Fig. 2 is a graph showing a relation between a channel body potential and word line voltage to explain an operational principle of the memory cell;
- [33] Fig. 3 is a diagram showing a band structure of the memory cell;
- [34] Fig. 4A is a diagram showing a structure of the memory cell using an FD-type MISFET according to a first embodiment (cell region);

- [35] Fig. 4B is a diagram showing the structure of the memory cell using the FD-type MISFET according to the first embodiment (peripheral region);
- [36] Fig. 5 is a diagram showing a basic band structure of the memory cell;
- [37] Fig. 6 is a diagram showing the band structure of the memory cell in a "0" state;
- [38] Fig. 7 is a graph showing a relation between a threshold voltage and an auxiliary gate voltage of the memory cell holding "0" data and "1" data;
- [39] Fig. 8 is a graph showing an operation waveform of "0" data write/read of the memory cell;
- [40] Fig. 9 is a graph showing an operation waveform of "1" data write/read of the memory cell;
- [41] Fig. 10 is a graph showing characteristics between a drain current and a gate voltage in a read operation of the memory cell;

- [42] Fig. 11 is a graph showing a relation between the threshold voltage and the auxiliary gate voltage of the memory cell holding "0" data and "1" data;
- [43] Fig. 12A is a diagram showing a structure of a memory cell according to a second embodiment (cell region);
- [44] Fig. 12B is a diagram showing the structure of the memory cell according to the second embodiment (peripheral region);
- [45] Fig. 13A is a diagram showing a structure of a memory cell according to a third embodiment (cell region);
- [46] Fig. 13B is a diagram showing the structure of the memory cell according to the third embodiment (peripheral region);
- [47] Fig. 14A is a diagram showing a structure of a memory cell according to a fourth embodiment (cell region);
- [48] Fig. 14B is a diagram showing the structure of the memory cell according to the fourth embodiment (peripheral region);

- [49]** Fig. 15 is a diagram showing a structure of a memory cell according to a fifth embodiment;
- [50]** Fig. 16A is a diagram showing a structure of a memory cell according to a sixth embodiment (sectional view taken along a bit line BL);
- [51]** Fig. 16B is a diagram showing the structure of the memory cell according to the sixth embodiment (sectional view taken along a word line WL);
- [52]** Fig. 17 is a graph showing an operation waveform of "0" data write/read of the memory cell;
- [53]** Fig. 18 is a graph showing an operation waveform of "1" data write/read of the memory cell;
- [54]** Fig. 19 is a graph showing characteristics between a drain current and a gate voltage in a read operation of the memory cell;
- [55]** Fig. 20A is a graph showing a relation between a threshold voltage and an auxiliary gate voltage of the memory cell holding "0" data and "1" data, when an intrinsic silicon is used as the channel body;

- [56] Fig. 20B is a block diagram showing a structure of a memory chip including a mimic transistor in addition to the memory cell array;
- [57] Fig. 21 is a diagram showing a specific layout of the memory cell array according to the cell structure of the first embodiment;
- [58] Fig. 22 is a sectional diagram taken along the line I-I' in Fig. 21;
- [59] Fig. 23 is a sectional diagram taken along the line II-II' in Fig. 21;
- [60] Fig. 24 is a sectional diagram taken along the line III-III' in Fig. 21;
- [61] Fig. 25 is a diagram showing a specific layout of the memory cell array according to the cell structure of the fifth embodiment;
- [62] Fig. 26 is a sectional diagram taken along the line I-I' in Fig. 25;

- [63] Fig. 27 is a sectional diagram taken along the line II-II' in Fig. 25;
- [64] Fig. 28 is a diagram showing a specific layout of the memory cell array according to the cell structure of the sixth embodiment;
- [65] Fig. 29 is a sectional diagram taken along the line I-I' in Fig. 28;
- [66] Fig. 30 is a sectional diagram taken along the line II-II' in Fig. 28;
- [67] Fig. 31 is a sectional diagram taken along the line III-III' in Fig. 28; and
- [68] Fig. 32 is a diagram showing an equivalent circuit of a memory chip including a memory cell array having the memory cells according to any one of the embodiments.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

- [69] Prior to an explanation of some embodiments, the case where a partial depletion type MISFET is used as a basic memory cell will be explained. In the partial depletion type MISFET, when a voltage is applied to a gate to form a

channel, a channel body is partially depleted and an electric neutral region remains therein. Such a MISFET is referred to as a PD-type MISFET hereinafter. Using the PD-type MISFET, it is possible to dynamically store a first data state in which excessive majority carriers are accumulated in the electric neutral region and a second state in which the excessive majority carriers in the electric neutral region are emitted.

[70] Fig. 1 shows the sectional structure of such a memory cell MC. The memory cell MC has an SOI substrate in which an insulating film 2 like a silicon oxide film is formed on a silicon substrate 1 and a p-type silicon layer 3 is formed on the insulating film 2. The silicon layer 3 is used as the channel body, a gate insulating film 4 is formed thereon, and source and drain diffusion regions 6 and 7 are formed in the silicon layer 3 deep to reach the insulating film 2, so that an n-channel MISFET is composed.

[71] Each memory cell MC composed of the n-channel MISFET has the channel body which is also element-isolated in a cross direction in a floating state, and the memory cells MC are arranged in the form of a matrix to constitute a cell array. The drain region 7 is connected to a bit line BL, the gate

5 is connected to a word line WL and the source region 6 is connected to a fixed potential line.

[72] The operational principle of the memory cell MC utilizes the accumulation of holes which are majority carriers in the channel body (the p-type silicon layer 3) of the MISFET. Specifically, a large electric current is sent from the drain region 7 by a pentode operating in the MISFET to generate impact ionization near the drain junction. Excessive holes which are majority carriers (holes) produced by this impact ionization are held by the channel body, and this state is defined, for example, as data "1". The state in which a forward current is sent between the drain region 7 and the channel body to emit the excessive holes in the channel body to the drain region 7 is defined as data "0".

[73] The data "0" and "1" are stored as potential difference in the channel body, that is, as difference in a threshold voltage of the MISFET. Namely, as shown in Fig. 2, a threshold voltage V_{th1} in a data "1" state in which the channel body potential V_{body} is high due to hole accumulation is lower than a threshold voltage V_{th0} in a data "0" state. In order to maintain the "1" data state

in which the holes are accumulated in the channel body, it is preferable that a voltage V_{WL} applied to the word line WL is kept in the negative. This data holding state is not changed even when a read operation is performed as long as the read operation is performed in a linear region and a write operation of inverted data is not performed. Namely, unlike the DRAM in which each memory cell has one transistor and one capacitor and which utilizes charge storage by the capacitor, non-destructive read-out is possible.

[74] Basically, reading data is performed to detect a difference of a conductivity of the memory cell MC. Since the relation between the word line voltage V_{WL} and the channel body potential V_{body} is shown in Fig. 2, for example, the word line WL is given a read voltage, which has an intermediate value between the threshold voltages V_{th0} and V_{th1} of the data "0" and "1", to detect whether or not a current is passed through the memory cell MC, whereby the data can be detected. Or, the word line voltage V_{WL} in excess of the threshold voltages V_{th0} and V_{th1} is given to the word line WL to detect whether the

current of the memory cell MC is large or small, whereby the data can be detected.

[75] The memory cell MC shown in Fig. 1 has the so-called PD-type MISFET in which the electric neutral region exists in the channel body region. Specifically, as describing a band diagram in Fig. 3, when the gate is supplied with the voltage V_{fg} ($=V_{th}$) for forming the channel, a depletion layer extends to the intermediate point of the channel body, the electric neutral region remains near the bottom of the channel body. In this case, according to a scaling rule that the thickness of the channel body region decreases along with a decrease of a design rule, an impurity concentration of the channel body also has to increase. In order to suppress a roll-off effect for a gate length (channel length) L in the threshold voltage of the MISFET, namely, in order to suppress a short channel effect, it is necessary to increase the impurity concentration of the channel body together with the decrease of the gate length L .

[76] However, a leak current in a pn junction increases exponentially with the impurity concentration of the channel body. There are a diffusion current, a generation

and recombination current and a thermal field emission current (G. Vincent, A. Chantre and D. Bois, "Electric Field Effect on the Thermal Emission of Traps in Semiconductor Junctions," J.Appl.Phys., 50, pp.5484-5487, 1979) in components of the leak current in the pn junction. The two formers of them, that is, the diffusion current and the generation and recombination current are components which decrease if the impurity concentration N_A increases. Because, the diffusion current decreases due to a reducibility of a concentration of minority carriers in the electric neutral region if the impurity concentration N_A increases, and the generation and recombination current decreases due to a reduction of the depletion layer width if the impurity concentration N_A increases. The last components is observed as the leak current because electrons in a deep level of the silicon band gap is emitted by thermal energy and then probability of contribution to conduction is increased by strong electric field in the depletion layer. Namely, it is due to a tunnel effect. According to this theory, since the leak current exponentially depends on the strength of the electric field, the leak current exponentially increases depending on the increase of impurity concentration N_A .

[77] In addition, a signal amount $\Delta V_{th} = |V_{th0} - V_{th1}|$, which is a difference between the threshold voltage V_{th0} in the "0" data cell and the threshold voltage V_{th1} in the "1" data cell, is defined by substrate bias effect. As the thickness t_{ox} of the gate oxide film is thinned to suppress the roll-off of the threshold voltage, the substrate bias effect becomes weaker. Therefore, it is necessary that the impurity concentration of the channel body is increased to secure the enough signal amount ΔV_{th} . In conclusion, securing the large signal amount is incompatible with improving characteristics of data holding.

[78] Therefore, in the following embodiments, the memory cell is composed of a full depletion type MISFET so as to suppress the leak current in a scale-down and secure good characteristics of data holding. In the full depletion type MISFET, the impurity concentration and the thickness of the channel body is set such that the channel body is fully depleted when a voltage is applied to the gate to form the channel. Such a MISFET is referred to as an FD-type MISFET hereinafter. In the memory cell having such an FD-type MISFET, a state, in which the channel body

is fully depleted by the electric field from a main gate and the majority carriers can be accumulated in a portion of a second side of the channel body by electric field from an auxiliary gate, is regarded as a thermal equilibrium state. Then, the memory cell can be stored dynamically a first data state in which the majority carriers are accumulated in the portion of the second side of the channel body and a second data state in which the majority carriers in the portion of the second side of the channel body are emitted.

[79] [First embodiment]

[80] Figs. 4A and 4B show a memory cell structure according to a first embodiment using the FD-type MISFET. The memory cell MC has an SOI substrate in which an insulating film 12 like a silicon oxide film is formed on a silicon substrate 11 and a p-type silicon layer 13 is formed on the insulating film 11. Since the insulating film 12 is buried under the silicon layer 13, the insulating film 12 is referred to as a BOX (buried oxide) layer hereinafter. The memory cell MC is an n-channel MISFET and it has a main gate 15 formed on the p-type silicon layer 13 via a gate insulating film 14 and source and drain diffusion regions

16 and 17 which are formed with a self-aligned process using the main gate 15 and reach to the bottom of the silicon layer 13.

[81] As described in the concrete later, the p-type silicon layer 13 has an acceptor concentration N_A and a thickness such that it is fully depleted when a gate voltage is applied to the main gate 15 to form a channel in its surface. More specifically, the thickness of the depletion layer extended from the surface of the p-type silicon layer 13 can be expressed as $(4\epsilon_{Si} \cdot \phi_F / q \cdot N_A)^{1/2}$, where the ϕ_F is Fermi-potential and the ϵ_{Si} is a dielectric constant of silicon. Thus, condition of the full depletion type MISFET is $(4\epsilon_{Si} \cdot \phi_F / q \cdot N_A)^{1/2} > t_{Si}$.

[82] Furthermore, in the example of Figs. 4A and 4B, the silicon substrate 11 is p-type and an n^+ -type diffusion layer 18 is formed between the silicon substrate 11 and the BOX layer 12. The n^+ -type diffusion layer 18 is an auxiliary gate to apply a predetermined electric field to the back face of the channel body composed of the p-type silicon layer 13 by capacitive coupling. The n^+ -type diffusion layer 18 is formed as a common gate (back plate) at least throughout the cell array region. The case where a

negative bias voltage is applied to the channel body from its back face is considered herein, so that the n^+ -type diffusion layer 18 is formed as the auxiliary gate. However, the n^+ -type diffusion layer 18 is not formed, but the silicon substrate 11 may be used as the auxiliary gate in itself. Or, a p^+ -type diffusion layer may be formed as the auxiliary gate.

[83] The memory cells MC are arranged in the form of a matrix so as to isolate each channel body from one another in a width direction in a floating state, too. The n^+ -type diffusion layer 18 being the auxiliary gate is formed throughout the cell array region. In a peripheral region of the cell array region, the n^+ -type diffusion layer 18 is connected to an auxiliary gate terminal thereabove via a contact plug 20, which is a polysilicon or the like and embedded in the BOX layer 12 and an interlayer insulating film 19 formed on the n^+ -type diffusion layer 18.

[84] In one of the concrete examples, the gate length is $L=70$ nm, the thickness of the gate insulating film 14 is $t_{ox}=10$ nm, the acceptor concentration of the p-type silicon layer 13 (channel body) is $N_A=1.0 \times 10^{15} \text{ cm}^{-3}$, approximately. This acceptor concentration is very low. The thickness

of the silicon layer 13 is $t_{Si}=25$ through 50 nm, approximately. The BOX layer 12 has the thickness of 30 through 50 nm, and it is relatively thin in order to be easy to apply the electric field to the channel body from its back face.

[85] The memory cell under this condition becomes the FD-type MISFET. Fig. 5 shows a band structure when a surface channel is formed by contrast with Fig. 3. As shown in Fig. 5, the channel body is fully depleted when the voltage applied to the main gate is $V_{fg}=V_{th}$. However, this diagram shows the case where the p-type silicon substrate 11 directly contacts on the BOX layer 12. Under the circumstance that such a full depletion condition is met, a bias voltage V_{bg} is applied to the channel body from the auxiliary gate, so that a state in which holes can be accumulated in the portion of the back side face of the channel body fully depleted is established. In other words, the channel body is fully depleted by the electric field from the main gate and then the bias voltage V_{bg} is applied to the channel body by the auxiliary gate to realize the state in which a hole accumulating layer (p-type accumulated layer) is formed in the portion of the

back side face of the channel body. Fig. 6 shows this state by contrast with Fig. 5.

[86] As shown in Fig. 6, the voltage V_{fg} on the main gate and the voltage V_{bg} on the auxiliary gate fully deplete the channel body to form the state in which holes can be accumulated in the bottom portion of the channel body, and then this state is regarded as the "0" state of the memory cell. As time passed by, this "0" state is moved into a thermal equilibrium state in which holes are accumulated in the bottom portion of the channel body, and then it is defined as the "1" data holding state. For writing the "0" data, a forward current is sent between the drain region and the channel body to form a state in which the holes in the channel body are emitted (that is, a non-equilibrium state in which the channel body is fully depleted). For writing the "1" data in the "0" data cell, the impact ionization is generated by a pentode operation to form a state in which the holes are accumulated in the bottom of the channel body.

[87] Next will be consideration to the threshold voltage of the memory cell according to this embodiment. Under the state in which the silicon layer 13 is fully depleted by electric

field from the main gate, when the voltage V_{bg} is supplied to the auxiliary gate to lower the potential of the back face of the silicon layer 13 contacted to the BOX layer 12, the state accumulating the majority carriers (the holes in this case) can be obtained. Since there is no capacitive coupling from the auxiliary gate to the channel body because of fixed potential of the back face of the silicon layer 13, the threshold voltage V_{thacc} of the surface channel of the MISFET in this state is expressed by the following equation (1).

$$V_{thacc} = \phi_{FB} + (1 + C_{si}/C_{ox}) \cdot 2\phi_F - Q_{dep}/2C_{ox} - (C_{si}/C_{ox}) \cdot \phi_{bs} \quad \dots(1)$$

- [88]** Where, the ϕ_{FB} is a flat band voltage between the main gate 15 formed of the n-type polysilicon and the p-type silicon layer 13 (channel body) in the MOS structure, the ϕ_F is Fermi-potential, the ϕ_{bs} is a potential of the back face of the channel body, the C_{si} is a capacitance of the channel body ($=\epsilon_s/t_{Si}$), the C_{ox} is a capacitance of the gate insulating film ($=\epsilon_{ox}/t_{ox}$) and the Q_{dep} is a space charge amount of the channel body fully depleted ($=-q \cdot N_A \cdot t_{Si}$).

[89] On the other hand, under the state in which the auxiliary voltage V_{gb} necessary for accumulating the majority carriers (holes) in the back face of the silicon layer 13 is not applied to the channel body, since the silicon layer 13 is fully depleted, the threshold voltage of the surface transistor has influence of the capacitive coupling by the auxiliary gate from the back face of the silicon layer 13. Namely, the threshold voltage is changed depending on the thickness t_{BOX} of the BOX layer 12 and the value of the auxiliary gate voltage V_{bg} . If the threshold voltage in this case is V_{thdep} , it is expressed by the following equation (2).

$$V_{thdep} = V_{thacc} - (C_{box}/C_{ox}) / (1 + C_{box}/C_{si}) \cdot (V_{bg} - V_{bgacc}) \dots (2)$$

[90] Here, the voltage V_{bgacc} is a value of the auxiliary gate voltage V_{bg} necessary for accumulating the majority carriers in the portion of the back face of the silicon layer 13, and it is expressed by the following equation (3).

$$V_{bgacc} = \phi_{FB} - C_{si}/C_{box} \cdot 2 \phi_F - Q_{dep}/2C_{box} + (1 + C_{si}/C_{box}) \cdot \phi_{bs} \dots (3)$$

[91] Where, the ϕ_{bs} is a potential of the back face of the silicon layer 13. However, in the thermal equilibrium state in which the majority carriers (holes) are accumulated and settled, the ϕ_{bs} is 0 V. This state is a stable state obtained by applying the voltage necessary for fully depleting the silicon layer 13 to the main gate and the voltage V_{bgacc} to the auxiliary gate. In other words, this is also a state in which the "1" data is written with the pentode region operation of the memory cell and the generation of the majority carriers.

[92] On the other hand, in the state in which the "0" data is written, specifically, in the state shifted from the thermal equilibrium state by forwardly biasing the pn junction between the bit line and the channel body and then emitting the majority carriers (holes) accumulated, the potential ϕ_{bs} of the portion of the back face of the silicon layer 13 is not 0 V but negative value. In this state, the potential ϕ_{bs} of the back face of the silicon layer 13 in the "0" data state is assumed to be $\phi_{bs0} = -1.57 \times \phi_f$ in accordance with the result of the device simulation.

- [93] If a relation between the threshold voltage V_{th} and the auxiliary gate voltage V_{bg} is found out using the equations mentioned above, the result of Fig. 7 can be obtained, where $t_{ox}=10$ nm, $t_{BOX}=30$ nm, $t_{Si}=25$ nm, $NA=1.0 \times 10^{15}$ cm⁻³ and temperature is room one.
- [94] As shown in Fig. 7, when the V_{bg} is in the positive side more than -3V, since the majority carriers are not accumulated in the portion of the back face of the silicon layer 13, the channel body is fully depleted and a memory function is not realized. Specifically, even if the "1" data writing operation is performed and the majority carriers are generated, the majority carriers are not accumulated and then they are emitted to the source region 16 or the drain region 17 immediately.
- [95] As the V_{bg} goes to negative side more than -3V, the majority carriers (holes) can be accumulated by the electric field from the auxiliary gate side and the memory function can be realized gradually. From another viewpoint, this means that the memory cell structure keeps the stable state (full depletion state) in which the non-equilibrium state cannot exist when the V_{bg} is larger than -3V whereas the memory cell structure is in unstable state in which the

non-equilibrium state can exist when the V_{bg} is more negative than $-3V$. It can be said that a system including this non-equilibrium state is used as the DRAM cell in this embodiment. That is, the state to hold the "1" data is the thermal equilibrium state. The "0" data state (in which threshold voltage V_{th} is high) is the non-equilibrium state in which at least a part of the accumulated majority carriers is emitted, and this state is the unstable state which will return to the "1" data if it is held for a long time.

[96] If a memory operation is performed in a state where the auxiliary gate voltage V_{bg} is low enough and the majority carriers are accumulated for the "0" data and the "1" data, the signal amount ΔV_{th} is expressed by the following equation (4) on the basis of the equation (1).

$$\Delta V_{th} = (C_{si}/C_{ox}) \cdot \Delta \phi_{bs} \quad \dots(4)$$

[97] Here, the $\Delta \phi_{bs}$ is a potential difference in back face of the silicon layer 13 between the "0" data state and the "1" data state. Thereby, it is understood that the ratio of the C_{si} to the C_{ox} namely t_{ox}/t_{si} may be larger or the

$\Delta \phi_{bs}$ may be larger in order to increase the signal amount. The former is condition of the device structure and the latter means signal becomes large if the potential of the bit line is negative enough on the "0" data writing operation.

[98] As being apparent from the equation (4), in the memory cell according to this embodiment, the signal amount does not depend on the impurity concentration of the channel body, and it is different from the memory cell using the PD-type MISFET. The conditions that the signal amount increases as the Cox is smaller namely the thickness tox of the gate oxide film is thicker is the same. However, the PD-type MISFET has a large short channel effect, so that the tox cannot be thickened.

[99] In contrast, in this embodiment using the FD-type MISFET, since the short channel effect is greatly improved, the tox can be thickened. Furthermore, viewed in the structure, the fact that the signal amount depends on only tox/tsi means that the signal amount can be kept constant if this ratio remains even though the channel length is more shortened in the future. Hence, it indicates that the scale-down is possible.

- [100] The followings are an actual result of the two-dimensional device simulation for verification of the memory operation. The device parameters are the gate length $L=70\text{nm}$, the gate oxide film thickness $t_{\text{ox}}=10\text{nm}$, the BOX layer thickness $t_{\text{BOX}}=30\text{nm}$, the silicon layer thickness $t_{\text{si}}=25\text{nm}$, the acceptor concentration $N_A=1.0\times 10^{15}\text{cm}^{-3}$ and the $V_{\text{bg}}=-5\text{V}$.
- [101] Fig. 8 shows a diagram in the case where the "0" read operation subsequent to the "0" write operation is performed, and Fig. 9 shows a diagram in the case where the "1" read operation subsequent to the "1" write operation is performed. As shown in Fig. 8, the gate voltage is raised from -4V to 1V , and next, the drain voltage is lowered from 0V to -1.5V , so that the "0" data write operation is performed. Then, the gate voltage is returned to -4V and the drain voltage is returned to approximately 0V at timing of $2.5\text{E}-08$. This timing indicates the data holding state and then the read operation is performed with raising the gate voltage again.
- [102] As shown in Fig. 9, the gate voltage is raised from -4V to 1V , and next, the drain voltage is raised from 0V to

1.5V, so that the "1" data write operation is performed. Then, the gate voltage is returned to -4V and the drain voltage is returned to approximately 0V at timing of $2.5\text{E}-08$. This timing indicates the data holding state and then the read operation is performed with raising the gate voltage again. The source voltage (fixed potential line voltage) is 0V in both cases.

[103] In Figs 8 and 9, the body potential indicates quasi-Fermi potential of holes in the center of the channel body (in the center of the channel length direction and the silicon depth direction). Fig. 10 is a diagram showing characteristics of the drain current I_d versus gate voltage V_{gs} of the "0" data read operation and "1" data read operation, where I_{ds0} indicates characteristics of the "0" data read operation and I_{ds1} indicates characteristics of the "1" data read operation.

[104] Judging from the above-result, it is understood that the enough signal amount can be secured because the signal amount ΔV_{th} is approximately 500mV in the data read operations.

[105] Fig. 11 shows a dependency of the auxiliary gate voltage V_{bg} concerning the V_{th0} in the "0" data and the V_{th1} in the "1" data, and this is obtained by the same device simulation with the auxiliary gate voltage V_{bg} changed. This coincides with Fig. 7 of theoretical calculation.

[106] [Second embodiment]

[107] Figs. 12A and 12B shows a sectional structure of a memory cell MC according to a second embodiment by contrast with Figs. 4A and 4B. In this embodiment, a p^+ -type polysilicon layer 21 is buried under the BOX layer 12 as the auxiliary gate instead of the diffusion layer 18. In other words, the p^+ -type polysilicon layer 21 is an impurity doping layer between the semiconductor substrate 11 and the silicon layer 13. The p^+ -type polysilicon layer 21 may be formed as a common electrode at least throughout the cell array region.

[108] [Third embodiment]

[109] Figs. 13A and 13B show a memory cell structure according to a third embodiment by contrast with Figs. 12A and 12B. In this embodiment, the BOX layer 12 is thicker, and the

polysilicon layer (impurity doping layer) 21 is buried in the BOX layer 12 as the auxiliary gate. In this case, the p⁺-type polysilicon layer 21 may be formed as a common electrode at least throughout the cell array region.

[110] [Fourth embodiment]

[111] Figs. 14A and 14B shows a memory cell structure according to a fourth embodiment in which the structure of Figs. 13A and 13B is slightly modified. In this embodiment, the polysilicon layer 21 buried in the BOX layer 12 is formed as a plate line (auxiliary word line) in the stripe form in parallel with the word line WL composed of the gate electrode 15. The polysilicon layer 21 is connected to a supply terminal of the auxiliary gate voltage V_{bg} via the contact plug at the end portion of the word line direction, for example, at the end portion opposite to the side where a word line driver is arranged.

[112] In addition, the structure shown in Figs. 14A and 14B in which the auxiliary gates are separated from one another can be also applied to the diffusion layer 18 in Figs. 4A and 4B of the first embodiment, the polysilicon layer 21

in Figs. 12A and 12B and Figs. 13A and 13B of the second and third embodiments.

[113] [Fifth embodiment]

[114] In the embodiments mentioned above, although a lateral transistor in which the channel is formed in parallel with the substrate face is used as the MISFET, a vertical transistor in which the channel is formed perpendicular to the substrate face may be used. A sectional structure of a portion of two memory cells in such a manner is shown in Fig. 15.

[115] An n-type layer 32 is formed on an entire surface of a p-type silicon substrate 31, pillar shaped p-type silicon portions 33 are patterned and formed in each memory cell region on the n-type silicon layer 32. The p-type silicon layer 32 is a common source for all the memory cells. A main gate 36 is formed via a gate insulating film 35 on the one vertical side of the silicon portion 33 whereas an auxiliary gate 38 is formed via a gate insulating film 37 on the other vertical side thereof. Here, the case where the auxiliary gate 38 is shared by neighboring memory cells MC is shown. The main gate 36 and the auxiliary gate

38 are continuously formed in one direction in parallel as a word line WL and a plate line PL, respectively. A drain diffusion region 34 is formed in the top portion of each p-type silicon portion 33. A bit line 41 connected to each drain region 34 is provided on an interlayer insulating film 40.

[116] In this embodiment, the thickness of the p-type silicon portion 33 (width of lateral direction in this drawing) and the impurity concentration is chosen so as to be the FD-type MISFET, thereby the same operation as the above-mentioned embodiments can be realized.

[117] [Sixth embodiment]

[118] Figs. 16A and 16B also show sectional views of a vertical MISFET, however, the auxiliary gate for controlling the potential of the portion of the back side face of the channel body is not directly opposite to the back side face thereof, but a pair of auxiliary gates are opposite to each other at the bottom portion of the both side faces. It is the same as Figs. 4A and 4B that the n⁺-type diffusion layer 18 is formed under the BOX layer 12, but the BOX layer 12 is thicker. Therefore, as shown in Fig. 16B showing

the sectional view taken along the word line WL, polysilicon portions 22 are buried in the BOX layer 12 so as to be opposite to each other via gate insulating films 23 in the bottom portion of the p-type silicon layer 13. In this embodiment, the polysilicon portions 22 are buried on both sides of the p-type silicon layer 13, and the bottom of the polysilicon portions 22 are connected to the n⁺-type diffusion layer 18. As a result, the polysilicon portions 22 are auxiliary gates for controlling a potential of the bottom portion of the p-type silicon layer 13 with capacitive coupling.

[119] In this embodiment, it is verified by the simulation that the same memory operation as the above-mentioned embodiments can be realized. The followings are a result of a three-dimensional device simulation. Parameters are that the gate length L and gate width W are 0.175 μm , the gate oxide film thickness tox_f of the main gate 15 side is 6.5 nm, the acceptor concentration N_A of the channel body is $1.0 \times 10^{15} \text{cm}^{-3}$, both the main gate 15 and the auxiliary gate 22 are the n⁺-type polysilicon, the auxiliary gate voltage V_{bg} is -4V, the gate oxide film thickness tox_b of the auxiliary gate side is 15nm, the

thickness t_{Si} of the silicon layer 13 is 140nm and the BOX layer thickness is 200nm. The polysilicon portions 22 are buried up to the middle height of the channel body.

[120] Figs. 17 and 18 show operating waveforms of the "0" data write/read and the "1" data write/read and correspond to Figs. 8 and 9 in the first embodiment, respectively. Fig. 19 shows characteristics of the drain current I_{ds} versus the gate voltage V_{gs} in the read operation and corresponds to Fig. 10. In this embodiment, the signal amount $\Delta V_{th}=250mV$.

[121] [A MISFET having an intrinsic silicon as the channel body]

[122] In the above-mentioned embodiments, n-channel MISFET having the channel body of p-type silicon is used. On the other hand, it is possible that a MISFET having the channel body of an intrinsic silicon which does not substantially include impurity. That way, there is no leak current caused by crystalline unconformity in the channel body because of impurity diffusion and so on, so that data holding characteristics are improved further. In order that the threshold voltage V_{th} of the MISFET is positive, it is necessary to use p⁺-type polysilicon for the main

gate. However, even if the threshold voltage is negative, it is enough that the operation is performed in the condition that the word line level is lowered by approximately 1V, so that an n⁺-type polysilicon may be used for the main gate.

[123] Fig. 20A shows a calculation result of a relation of the threshold voltages V_{th0} and V_{th1} in the "0" data and "1" data versus the auxiliary gate voltage V_{bg} in the case where the intrinsic silicon is used as the channel body in the MISFET, by contrast with the Fig. 11. Here, the assumption is made that the p⁺-type polysilicon is used for the main gate.

[124] The value of the auxiliary gate voltage V_{bg} must be in the negative side more than the value capable of accumulating the majority carriers in the channel body of the "1" data cell. Furthermore, if the value of the auxiliary gate voltage V_{bg} is in the negative side more than the value ($V_{bg} = -2V$ in Fig. 20A) capable of accumulating the majority carriers in the channel body of the "0" data cell, the signal amount ΔV_{th} is maximized. However, it is important that the electric field in the junction between the drain and the source in the channel body in the "0"

data cell is reduced in order to increase data holding time. From the viewpoint of this, it is preferable that the back face potential of the channel body in the "0" data cell is not lowered by a large amount in a negative direction but the channel body is in the full depletion state in which the majority carriers are not accumulated. For this purpose, the auxiliary gate voltage V_{bg} may be set between the value at which the majority carriers are accumulated in the channel body in the "1" data cell and the value at which the majority carriers are accumulated in the channel body in the "0" data cell. In accordance with the result of Fig. 20A in this embodiment, it is set in the range of $-2.0V < V_{bg} < 0.5V$. However, if the data holding time is set longer than required specification, it is preferable that the voltage V_{bg} is set at the value smaller than the value capable of accumulating the majority carriers in the channel body in the "0" data cell and then the signal amount is maximized.

[125] [Fluctuation of device parameters in the above-mentioned embodiments]

[126] Next, the following Table 1 shows characteristic changes owing to fluctuation of various device parameters when the

DRAM according to the above-mentioned embodiment is manufactured.

Table 1

| sample No. | 0 | 1 | 2 | 3 | 4 | 5 | 6 |
|-----------------------|-------|-------|-------|-------|-------|-------|-------|
| NA[cm ⁻³] | 1E+15 | 1E+15 | 1E+15 | 1E+15 | 1E+15 | 1E+15 | 1E+15 |
| tox[nm] | 10 | 10 | 10 | 10 | 10 | 8 | 12 |
| tBOX[nm] | 30 | 30 | 30 | 20 | 40 | 30 | 30 |
| tSi[nm] | 25 | 15 | 35 | 25 | 25 | 25 | 25 |
| Vbg0[V] | -5 | -7.5 | -4 | -4 | -6.5 | -5 | -5 |
| Vbg1[V] | -3 | -4.5 | -2.25 | -2 | -3.5 | -3 | -3 |
| Vbgs[V] | -4.5 | -6.75 | -3.56 | -3.5 | -5.75 | -4.5 | -4.5 |
| Vth0[mV] | 1050 | 1800 | 710 | 1100 | 1050 | 810 | 1290 |
| Vth1[mV] | 620 | 1100 | 410 | 610 | 610 | 490 | 780 |
| ΔV_{th} [mV] | 430 | 700 | 300 | 490 | 440 | 320 | 510 |

[127] In the Table 1, since the fluctuation of the channel length L and the acceptor concentration NA of the channel body has little influence, these changes are ignored. Except for this, to the changes of the gate oxide film thickness tox, the BOX layer thickness tBOX and silicon layer thickness tSi, the Vbg0 indicates the maximum auxiliary gate voltage necessary for accumulating the majority carriers (holes) in the channel body in the "0" data cell, whereas the Vbg1 indicates the maximum auxiliary gate voltage necessary for accumulating the majority carriers (holes) in the channel body in the "1" data cell. In

addition, the actual setting voltage of the auxiliary gate voltage V_{bgs} is calculated by $V_{bgs} = V_{bg0} + (V_{bg1} - V_{bg0}) \times 0.25$, under the condition that the channel body is fully depleted on the "0" data holding on the basis of conditions for acquiring large signal amount. Table 1 further shows the threshold voltage V_{th0} of the "0" data cell, the threshold voltage V_{th1} of the "1" data cell and the difference ΔV_{th} therebetween then.

[128] As shown in Table 1, when the changing conditions are $t_{ox} = 10\text{nm} \pm 20\%$, $t_{BOX} = 30\text{nm} \pm 33\%$ and $t_{Si} = 25\text{nm} \pm 40\%$, the optimum setting voltage V_{bgs} of the auxiliary gate is changed in the range of -3.5V through -6.75V. Moreover, the threshold voltage V_{th0} of the "0" data cell is changed in the range of 710mV through 1800mV whereas the threshold voltage V_{th1} of the "1" data cell is changed in the range of 410mV through 1100mV

[129] It must be important to suppress these changes. In the examples above, although the changes are intentionally emphasized, there is a possibility of the changes in the range of approximately $\pm 10\%$ in fact. In such a precondition, even if there are these changes, it is also important to adjust the auxiliary gate voltage V_{bgs} , a high

level voltage VWLHW of the word line on the write operation, a voltage VWLHR of the word line on the read operation and a low level voltage VWLL of word line on the holding state, last three being necessary to be adjusted by the changes of the threshold voltages V_{th0} and V_{th1} , through the chip selecting test. Since it can be considered that there is no these parameter changes in one chip, the adjusting (trimming) for each chip is enough. Or, the adjusting for wafer unit or lot unit may be enough in some cases. The influence on sense amplifiers in the read operation is unimportant, because the changes of the V_{th} are canceled each other as long as dummy cells having the same structure as the memory cell are used.

- [130]** There are various method for the adjusting of the auxiliary gate voltage V_{bgs} and the above-mentioned word line potential VWLHW/VWLHR/VWLL. For instance, a test MISFET having the same structure as the memory cell is provided for each chip. When the chip selecting test is performed, the "0" data write/read operation and the "1" data write/read operation are performed to/from the test MISFET, and then the threshold voltages V_{th0} and V_{th1} are measured in a triode region of the test MISFET. The same

tests are repeated with the auxiliary gate voltage V_{bg} changed, and the optimum auxiliary gate voltage V_{bg} is decided.

[131] Fig. 20B is a diagram showing such a chip structure. As shown in Fig. 20B, the chip has a mimic transistor 90 in addition to a memory cell array 80. The mimic transistor 90 has the same structure as the memory cells MC in the memory cell array 80. However, there are difference points that its main gate MG, source region S, drain region D and auxiliary gate AG are connected to pads 92, 94, 96 and 98, respectively. That is, the chip has the pads 92, 94, 96 and 98 to test the mimic transistor 90.

[132] Therefore, the main gate voltage V_{fg} can be directly applied to the main gate MG from the pad 92, and the auxiliary gate voltage V_{bg} can be directly applied to the auxiliary gate AG from the pad 98. Moreover, by measuring a current flowing between the pad 94 and the pad 96, a current flowing between the source region S and the drain region D of the mimic transistor 90 can be directly measured. As a result, it is possible to write the "1" data into the mimic transistor 90 and the "0" data into the mimic transistor 90. Furthermore, it is possible to

easily measure the threshold voltage V_{th1} of the "1" data write state and the threshold voltage V_{th0} of the "0" data write state.

[133] Since the chip has the mimic transistor 90 of this structure, it is possible to accurately measure what voltage the auxiliary gate V_{bg} , what voltage the high level voltage V_{WLHW} of the word line on the write operation, the voltage V_{WLHR} of the word line on the read operation and the low level voltage V_{WLL} of word line on the holding state should be adjusted.

[134] On the other hand, a nonvolatile memory circuit like fuses is mounted on the memory chip as an initial setting data memory circuit to initially set operation conditions. Then, in accordance with the result of the above-mentioned test, the fuses are programmed. The programmed data are read when power is turned on, an auxiliary gate voltage setting circuit, a word line voltage generating circuit and so on for $V_{WLHW}/V_{WLHR}/V_{WLL}$ are initially set. In this manner, it is possible to set the optimum operation condition for each memory chip.

- [135] [Cell array structure in the first embodiment]
- [136] Fig. 21 shows a layout of a concrete cell array according to the first embodiment, and Figs. 22, 23 and 24 are sectional diagrams taken along the lines I-I', II-II' and III-III' in Fig. 21, respectively. As shown in Figs. 23 and 24, the p-type silicon layers 13 of the SOI substrate are defined as element forming regions in the form of stripes extending in the bit line direction by an element isolation insulating film 106, which is the STI (shallow trench isolation). Then, the MISFETs are formed and arranged such that the source region 16 and the drain region 17 in the each p-type silicon layer 13 are shared between neighboring MISFETs in the bit line direction, respectively.
- [137] The gate electrodes 15 are continuously formed as word lines WL in the direction intersecting the bit lines BL, specifically, perpendicular to the bit lines BL. The top face and both side faces are covered with silicon nitride film 101. In an interlayer insulating film 103 covering the elements, common source lines 102 (SL) are formed as polysilicon wirings and each common source line 102 is commonly connected to the source regions 16 of the MISFETs

arranged in the word line direction. Bit lines 105 (BL) are formed on the interlayer insulating film 103, and each bit line 105 is connected to drain regions 17 of the MISFETs. The n^+ -type layer 18 as the auxiliary gate is formed as a common electrode throughout the whole cell array.

[138] If the word lines WL and the bit lines BL are formed in line/space of the minimum feature size F , a unit cell area is $4F^2$ indicated by one dotted chain line in Fig. 21.

[139] [Cell array structure in the fifth embodiment]

[140] Fig. 25 shows a layout of a concrete cell array according to the fifth embodiment in which the basic cell structure is shown in Fig. 15, and Figs. 26 and 27 are sectional diagrams taken along the lines I-I' and II-II' in Fig. 25, respectively. A silicon wafer having p/n/p structure is used, and grooves whose depth reach the n-type layer 32 are formed, so that pillar type and p-type silicon portions 33 are formed and arranged. The insulating film 39 is buried in the grooves. Further grooves are formed in the insulating film 39 at the position where the word lines WL and the plate lines PL are buried, and the main gates

36 and the auxiliary gates 38 are buried at both sides of each silicon portion 33 such that the main gates 36 are opposite to the auxiliary gates 38 via the gate insulating films 35 and 37. As shown in Fig. 25, the main gates 36 and the auxiliary gates 38 are formed and patterned as word lines WL and plate lines (auxiliary word lines) PL in parallel with one another.

[141] Although the gate insulating films 35 and 37 are formed with the same process when the thickness of the gate insulating films 35 and 37 are the same, separate processes are needed when they have different thickness. The top face and the both side faces of the main gates 36 and the auxiliary gates 38 are covered with silicon nitride films 110. After the drain regions 34 are formed with a diffusion process in the top portions of the silicon portions 33, the interlayer insulating film 40 is deposited. Contact plugs 112 are buried in the interlayer insulating film 40, the bit lines 41 (BL) are provided on the interlayer insulating film 40, and then the cell array is constituted.

[142] As shown in Fig. 25, each plate line PL is arranged between two word lines WL and WL so as to be shared between two

neighboring memory cells in the bit line direction. In this embodiment, if the line/space of the word lines WL and the plate lines PL is F and the line/space of the bit lines BL is F, a unit cell area is $6F^2$.

[143] [Cell array structure in the sixth embodiment]

[144] Fig. 28 shows a layout of a concrete cell array according to the sixth embodiment in which the basic cell structure is shown in Fig. 16, and Figs. 29, 30 and 31 are sectional diagrams taken along the lines I-I', II-II' and III-III' in Fig. 28, respectively. The basic cell array structure of Figs. 28 and 29 is the same as that of Figs. 21 and 22. However, it is different that the polysilicon portions 22 are buried to constitute auxiliary gates in parallel with the bit lines BL at each position between bit lines BL and BL. As shown in Fig. 30, the polysilicon portions 22 are buried in the BOX layer 12 so as to be opposite to each other at the bottom side faces of each p-type silicon portion 13. In this embodiment, their top faces are located at the middle of thickness of the p-type silicon portions 13, so that they constitute the plate lines (auxiliary word lines) PL.

- [145]** [Equivalent circuit of the memory chip]
- [146]** Although the examples of the cell array structure are explained hereinbefore, an equivalent circuit of the memory chip including peripheral circuits is shown in Fig. 32. The word lines WL are the main gates in the memory cell array 201, and they are selectively driven by a row decoder (including a word line driver) 205. The bit lines BL are connected to a sense amplifier 202, and then the data write and the data read is performed between the bit lines of the column selected by a column decoder 203 and an I/O terminal via a data buffer 204.
- [147]** An address signal is input to an address buffer 206, a row address is decoded by the row decoder 205 and a column address is decoded by the column decoder 203.
- [148]** Various control signals applied to the word lines in the cell array 201 via the row decoder 205 and the auxiliary gate voltage Vbg applied to the auxiliary gate are generated by an internal voltage generating circuit 207 using a booster circuit and so on. As described above, the various control signals include a high level voltage VWLHW of the word line on the write operation, a voltage

VWLHR of the word line on the read operation and a low level voltage VWLL of word line on the holding state. An initial setting resistor 209 is provided in order to set an output voltage from the internal voltage generating circuit 207 at the optimum value in each chip.

[149] As mentioned above, in accordance with the test result, a fuse circuit 208 is provided as the nonvolatile memory circuit in order to set various voltages output from the internal voltage generating circuit 207 at the optimum value. According to the programming of the fuse circuit 208, initial setting values of the various voltages are decided. On the occasion of the memory operation, a power-on detecting circuit 210 detects a power-on and the data in the fuse circuit 208 is automatically read into the initial setting resistor 209 based on the output from the power-on detecting circuit 210. The internal voltage generating circuit 207 is controlled by the output from the initial setting resistor 209, so that the optimum control voltage VWL, the auxiliary gate voltage Vbg and so on are generated in each chip.